Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTION**

1. **OUTPUT A**
2. **INPUT A –**
3. **INPUT A +**
4. **V –**
5. **INPUT B +**
6. **INPUT B –**
7. **OUTPUT B**
8. **V+**

**.066”**

**.071”**

**1 8 7**

**6**

**5**

**2**

**3**

**4**

**DIE ID**

**LMC6482B**

**NOTE: Some damage may be visible near the probe-only pads**

**due to blown poly fuses used for VOS trim. Devices should not**

**be rejected for this reason.**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .004” X .004”**

**Backside Potential: V+ (can also be left floating)**

**Mask Ref: LMC6482B**

**APPROVED BY: DK DIE SIZE .066” X .071” DATE: 7/7/22**

**MFG: TEXAS / NATIONAL THICKNESS .015” P/N: LMC6482**

**DG 10.1.2**

#### Rev B, 7/19/02